What is claimed is:

1. An apparatus for solving key equation polynomials in decoding error correction codes, a novel inversionless decomposed architecture which is frequently used in BCH and Reed-Solomon decoders comprising:

a syndrome calculator that received codewords and output a syndrome polynomial to a key equation solver;

a key equation solver that calculated error locator polynomial and error evaluator polynomial and output error location ;

a Chein Search that received said error locator polynomial and input a result to an error value calculator and output said error location;

an error value calculator that received signal from said key equation solver and Chein Search ,output an error value.

2. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus is used for BCH and Reed-Solomon (RS) decoders.

3. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus is applied to BCH and Reed-Solomon (RS) decoders which is a kind of inversionless decomposed architecture.

4. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus can be applied to the correction of errors as well as erasures.

5. An apparatus for solving key equation polynomials in decoding error correction codes in claim 1,wherein said method and apparatus is applied in inversionless Euclidean.

6. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus can eliminate the finite-field inverter (FFI) to finish.

7. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus is only

needed t iteration decoding procedure.

8. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus including said decomposed technique which can also drastically reduce the required number of finite-field multipliers (FFMs) from 4t~6t to 3.

9. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus including said decomposed technique that uses only $4t+2\rho+4$ registers.

10. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus including said decomposed technique that no FFIs is presented to implement the inversionless Euclidean algorithm.

11. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus can use to calculate the Forney syndrome polynomial.

12. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said apparatus is further operable in communication.

13. A method for solving key equation polynomials in decoding error correction codes. In particular, a novel method for inversionless decomposed architecture which is frequently used in BCH and Reed-Solomon decoders executable instructions for::

(a) received said codewords and calculate said syndrome;

(b) produced said errata locator polynomial and errata evaluator polynomial;

(c) search said error location;

(d) calculated said error value.

14. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method is used for BCH and Reed-Solomon (RS) decoders.

15. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method is applied to

BCH and Reed-Solomon (RS) decoders which is a kind of inversionless decomposed architecture.

16. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method can be applied to the correction of errors as well as erasures.

17. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method is applied in inversionless Euclidean.

18. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method can eliminate the finite-field inverter (FFI) to finish.

19. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method is only needed t iteration decoding procedure.

20. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method including said decomposed technique which can also drastically reduce the required number of finite-field multipliers (FFMs) from 4t~6t to 3.

21. An apparatus for solving key equation polynomials in decoding error correction codes according to claim 1,wherein said method including said decomposed technique that uses only $4t+2\rho+4$ registers.

22. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method including said decomposed technique which no FFIs is presented to implement the inversionless Euclidean algorithm.

23. A method for solving key equation polynomials in decoding error correction codes according to claim 13,wherein said method including said decomposed technique which can also use to calculate the Forney syndrome polynomial.

24. A method for solving key equation polynomials in decoding error

correction codes according to claim 13,wherein said method and apparatus is further operable in communication.

25. A method for solving key equation polynomials in decoding error correction codes. In particular, a novel method for inversionless decomposed architecture which is frequently used in BCH and Reed-Solomon decoders, wherein improving process including;
(a) improved the speed of said Educlidean algorithm;
(b) embellished said decoded procedure to reduce half decoded result;
(c) combined the calculate which said errata locator polynomial and errata evaluator polynomial.

26. A mothed as recited in claim 25,wherein said Educlidean algorithm and time is shared said finite-field multipliers (FFMs).

27. A mothed as recited in claim 25,wherein said method can reduce said hardware area.

28. A mothed as recited in claim 25,wherein said modified Educlidean algoridean is a decomposed architecture, eliminated the limit of finite-field inversionless

29. A mothed as recited in claim 25,wherein said inversionless Educlidean algoridean including total iteration number of degree is less than t but also other architectures requires at most 2t interations.

30. A mothed as recited in claim 28,wherein said inversionless Educlidean algoridean use the degree of said error locator polynomial increase from $\rho+1$ to $\rho+t$.

31. A mothed as recited in claim 25,wherein said inversionless Educlidean algoridean ,the number of total iterations in our modified procedure is less than t.

32. A method for solving key equation polynomials in decoding error correction codes. In particular, a novel method for inversionless decomposed architecture which is frequency used in BCH and Reed-Solomon decoders including:

(a) each iteration could eliminate at least one degree;
(b) combined the hardware of said errata locator polynomial and errata evaluator polynomial;
(c) a number of FFMs is reduced to 3.

33. A mothed as recited in claim 32,wherein said speed of inversionless Educlidean algoridean slowing down, but it will not impact the decoding speed.

34. A mothed as recited in claim 32,wherein said BCH and Reed-Solomon (RS) decoder,Digital Versatile Disks (DVDs) use a RS product code which is (182,172)in the row direction and (208,192)in the column direction.

35. A mothed as recited in claim 32,wherein said BCH and Reed-Solomon (RS) decoder, digital TV broadcasting uses a (204,188) RS code.

36. A mothed as recited in claim 32,wherein said BCH and Reed-Solomon (RS) decoder, CD-ROM uses a number of smaller RS codes, including (32,28),(28,24).

37. A mothed as recited in claim 32,wherein said BCH and Reed-Solomon (RS) decoder, in wireless communications, the AMPS cellular phone system uses (40,28) and (48,36) binary BCH codes, which are shortened codes of the (63,51) code.